95. The device according to claim 94, wherein the reset circuit includes a tag register associated with individual ones of the blocks such that those blocks having their tag registers set are simultaneously reset while those blocks not having their tag registers set are not reset.

96. The device according to claim 92, additionally comprising means for substituting a redundant block of cells for a defective one of said blocks of cells.

97. The device according to claim 92, wherein said memory device interfaces with a host computer to receive the stored data grouped in magnetic disk drive sectors of data.

98. The device according to claim 63, further comprising a cache memory connected to store hold the stored data prior to it being programmed int said memory cells.--

REMARKS

It is respectfully requested that an interference be declared between the present application and patent 5,657,270 of Ohuchi et al. (hereinafter referred to as the "'270 patent"). Claim 63 of the present application corresponds exactly to claim 1 of the '270 patent. Claim 63 is suggested as the count for the interference, as follows:

Count 1

A non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said

memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.

35 U.S.C. 135(b)

Claim 63 of the present application was added by Preliminary Amendment, simultaneously with the filing of the present application on August 5, 1998. This is less than one year after the `270 patent was granted on August 12, 1997.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by the Preliminary Amendment filed on August 5, 1998, the present application is entitled to an effective filing date of April 13, 1989.

The `270 patent is shown to have a United States filing date of January 23, 1995, claiming priority from a chain of United States continuation applications dating back to March 29, 1991, and two Japanese applications filed March 31, 1990 and September 25, 1990. Thus, the earliest priority date noted on the `270 patent is nearly one year later than the April 13, 1989 effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Support for the Proposed Count 1 in the Preliminary Amendment to the Present Application

(N.B. All references in the right hand column are with respect to the Preliminary Amendment.)

Count 1	Present Application (Preliminary Amendment)
A non-volatile semiconductor memory device comprising:	The embodiments described are non-volatile semiconductor devices.

a plurality of bit lines;	The described memory system embodiment has a plurality of bit lines 1091, 1093, ... in Figure 12, and as described, for example, at page 7, lines 24-30.
a plurality of word lines insulatively intersecting said bit lines;	The word lines are 1077, 1079, ... in Fig. 12 and described at p. 7, lns. 20-24. These intersect the bit lines, as also shown in figure 12. The details of this as "insulatively intersecting" can be seen in Fig. 9 and is described at p. 6, ln. 26 through p. 7, ln. 9, with an insulator, for example 1033, between word line 1027 and bit line 1019.
a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;	Fig. 12 shows the memory cell array, with cells coupled to bit lines and word lines, for example, cell 1063 coupled to 1091 and 1077. Fig. 9-11 show details of the cell with a floating gate, such as 1023, for charge storage. This is described at p. 6, lns. 1-17.
a plurality of programming circuits coupled to said memory cell array	The programming circuits are shown in Fig. 13 as 1190, 1200, 1210, and 1220. More detail is given in Fig. 22, showing them coupled to array 1060, and in Figs. 24 and 25, showing that they are a plurality. The description is at p. 19, ln. 1 through p. 21, ln. 28.

(i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells,	This storage occurs in latch 1721 of Fig. 24, which shows in more detail block 1200 of Fig. 13, and is described at p. 20, ln. 10 through p. 21, ln. 14 in conjunction with Fig. 23.
(ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits,	Block 1210 of Fig. 13 and Fig. 22, with description at p. 19, ln. 22 through p. 20, ln. 25 in conjunction with Figs. 23 and 24.
(iii) for determining actual written states of said memory cells, and	This occurs in the compare circuit of block 1200 of Fig. 13, shown in more detail in Fig. 24 and described at p. 20, ln. 26 through p.21, ln. 14.
(iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.	Block 1210 of Fig. 13 in conjunction with blocks 1190, 1200, 1210, and 1220, as mentioned above. The program inhibit feature is described in more detail in Figs. 24 and 25 with description at p. 20, ln. 26 through p. 21 ln. 28.

The general structure of the memory array can be seen from Figure 12 of the present application as including a standard arrangement of bit lines, word lines, and memory cells. These cells are shown in detail in Figures 9-11. The description of the array is given in the disclosure from page

6, line 1 through page 8, line 21 of the Preliminary Amendment that was filed with, and became a part of, the present application. This description of the cells and their arrangement is that of count 1.

The programming circuits recited in count 1 with the limitations (i)-(iv) are shown in Figure 13 as blocks 1190, 1200, 1210, 1220. Figure 22, and, particularly, Figures 24 and 25 show the relevant parts in more detail. The function of these circuits is explained at page 19, line 1 through page 21, line 28 under the general label of "Program Inhibit." It is this disclosure, along with the operation flow chart of Figure 23, that describes the programming circuit of count 1.

This is especially made clear in light of the Initial Determination by the Administrative Law Judge of the International Trade Commission ("ITC") with regard to Investigation No. 337-TA-382. This ITC proceeding resulted in claim 27 of related U.S. patent no. 5,172,338 being held valid and infringed. Sections III C and V.C. of this Initial Determination are the most pertinent to the present application, a copy of which is being filed herewith. In the present application, the numbers of the Figures are 8 higher than those of the corresponding Figures in the '338 patent, and the reference numbers are 1000 higher.

In particular, Section III.C pages 62-74 of that decision uphold the view that the present application's programming circuits are the same as those described in count 1. These pages relate to patent 5,172,338 of Mehrotra et al., the text and figures of its parent application having been incorporated into the present application by the Preliminary Amendment filed with the present application. The '338 patent is written to include multi-state memory, but also covers the use of binary memory cells as a simplified case. How the memory array and programming circuits described therein function, and, consequentially, relate to count 1, is described in detail in the opinion found on pages 62-74 of the ITC Initial determination. It is described more briefly here, where the references are again to the material incorporated into the present application by the earlier Preliminary Amendment.

Figure 13 is a schematic of the circuit, the memory array residing in block 1060 that is shown in more detail in figures 9-12. The programming circuits are in blocks 1190, 1200, 1210, and 1220. The compare circuit 1200 and inhibit circuit 1210 are shown in more detail in figures 24 and 25, respectively. Some comments need to made about figure 24 and its simplification in the binary memory case.

The compare circuit 1200 determines whether a memory cell is correctly programmed or not. For a binary memory cell, these two choices---correct or not---are in direct one to one correspondence with the two states of the memory cell. For a multi-state memory cell with more than two states, this one to one correspondence breaks down: one state is correct, but all the others are not. This more general (L+1) state possibility requires the L XOR gates 1711-1715 of figure 24. In the binary state case, L=1 and there is only the single XOR gate 1711. This also reduces the NOR gate 1717 to a simple inverter for this one bit per cell case.

The one way latch 1721 then stores the data which defines whether or not write voltages are applied to the cell. This process is then done in a iterative manner until programming is complete. The read circuits 1220 of Figure 13 read out the result of an iteration, which is then compared in compare circuit 1200, and programming repeated by circuit 1210 until the circuit 1200 decides the cell is programmed. When the cell is programmed, the data bit in the one way latch 1721 is changed and, as a result, that particular cell is no longer written to. The circuit 1190 contains the initial data on which cells are to be programmed. In the multi-state case this serves as a point of reference, but can be thought of as simply a -1st iteration in the binary case of one bit per cell since there the latch 1721 determines whether the cell has achieved the predetermined state.

For these reasons, it is submitted to be clear that claim 1 of the `270 patent is supported by the present application disclosure, first filed on April 13, 1989.

`270 Patent Prosecution File History

A review of the file history of the `270 patent reveals that patent no. 5,172,338 was cited but not applied during the `270 patent prosecution. The `338 patent was included on the Information Disclosure Statements dated April 1, 1995, and June 19, 1995, filed after the third Office Action. In both cases, the forms 1449 were initialed on January 16, 1996. The `338 patent is not discussed in any of the Office Actions or Amendments, only being listed on forms 1449 that were part of the Information Disclosure Statements.

Information Disclosure Statement

An Information Disclosure Statement is being prepared to include references cited in parents to the present application and in the `270 patent. It is expected that this Statement, with forms 1449 and copies of the references, will be filed within two weeks from the date hereof.

Added Claims

This opportunity is being taken to add claims 92-98, all dependent upon claim 63, to include other features of the present application disclosure not included in the originally presented claims 63-91.

Conclusion

A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned attorney is invited.

Dated: December 3, 1998

Respectfully submitted,

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